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Design of Low Power Bypassing-Based Multiplier Using Vhdl

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***Abstract**: In this paper a low power bypassing -based multiplier design is present, in which reduction in power is to be achieved in changed partial products of column bypassing multiplier as compared to column bypassing multiplier by exchange NOR gates with AND gates in the conventional multiplier I.e. in the design of conventional multiplier rather than AND gate, NOR gate is employed victimization DeMorgan's theorem. Compare with 32×32 bits typical (parallel array) multiplier and column bypassing multiplier, this planned system reduces power.*
***Keywords:** changed column bypassing multiplier, conventional multiplier.*

I. Introduction

Multiplication is a necessary operation in DSP application. For the multiplication of 2 unsigned n-bit numbers, the number $A=a_{n-1}\, a_{n-2}\ldots a_0$ and also the multiplier factor,$B=b_{n-1}\, b_{n-2}\ldots b_0$ the product, $P= P_{2n-1}\, P_{2n-2}\ldots ,P_0$ is depicted as the following equation:

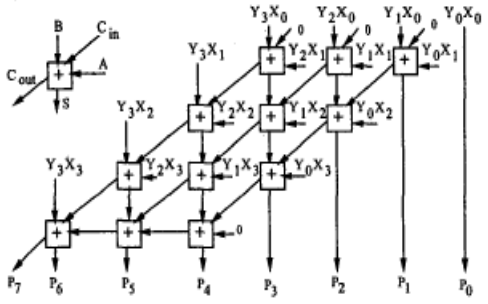
$$P= P_{2n-1}\, P_{2n-2}\ldots ,P_0 = \sum_{i=0}^{n-1}\sum_{j=0}^{n-1} (a_i\, b_j)\, 2^{i+j}$$

To achieve the superior demand in DSP application, the structure of parallel array multiplier factor is wide used and also the typical implementation of such Associate in Nursing array multiplier factor is Braun style. In n×n Braun multiplier[1],the multiplier factor array consists of (n-1) rows of carry-save adders(CSAs) and a (n-1) bit ripple carry adder within the last row, within which every row contains (n-1) Full adders(FAs). Multipliers square measure one among the foremost necessary arithmetic units in microprocessors and additionally a significant supply of power dissipation. Reducing the facility dissipation of multipliers is essential to satisfy the general power budged of varied digital circuits and system. Power consumed by multipliers is lowered at numerous levels of the planning hierarchy, from algorithmic rule to architectures to circuits, and devices. during this analysis work the planned system reduces the facility dissipation.

II. Preliminaries

A. Parallel array multiplier(Braun multiplier)

Array multiplier factor is documented as a result of its regular structure. multiplier factor circuit relies on add and shift algorithmic rule. every partial product is generated by the multiplication of the number with one multiplier factor bit. The partial product square measure shifted in line with their bit orders so else. The addition may be performed with traditional carry propagated adder. N-1 adders square measure needed wherever N is that the multiplier factor length. The implementation of parallel array multiplier factor is additionally known as as Braun design[5] as shown in figure1.



(a)

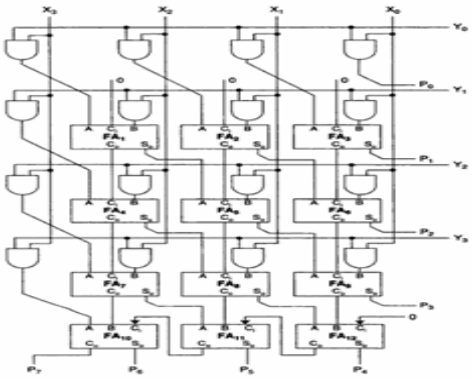
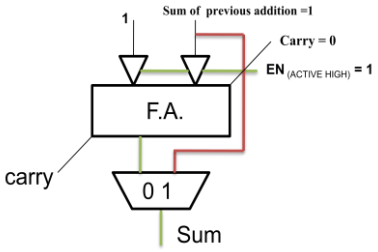


Figure 1:(a)multiplier arry,(b) Braun design

B. Low Power Bypassing Based Multiplier

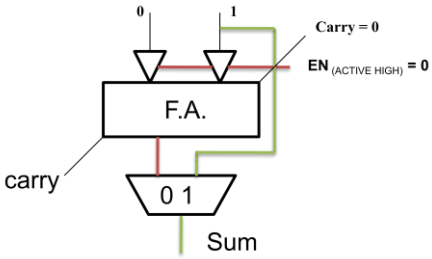
Column bypassing multiplier:

In column bypassing multiplier[4]. The unnecessary addition of zero bit is avoid and thus the switching power will saved. Also the advantage of this design is that it maintains original array structure without introducing extra circurcitary. Architecture is shown in figure 2.There are two cases involves in column bypassing: *Case 1:* As we are using active high buffer ,Adder will perform the addition only when buffer is active i.e. EN = 1.Hence no bypassing is done.



(a)

Case 2: If EN = 0 then Buffer remains deactivated and therefore the i/p applied get directly bypass.



(b)

Figure 2:(a)case1 (b)case 2

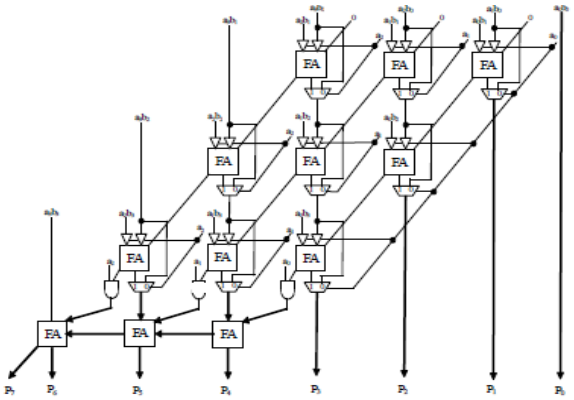


Figure 3: 4×4 braun multiplier with column bypassing

III. The Proposed Design

Modified column bypassing multiplier:

[3] We propose a multiplier design in which columns of adders are bypassed. In this approach, the operations in a column can be disabled if the corresponding bit in the multiplicand is 0. There are two advantages to this approach. First, it eliminates the extra correcting circuit as shown in Fig. 2. Secondly, the modified FA is simpler than that used in the row-bypassing multiplier[2]. In the second multiplier design instead of using AND gate we are using OR gate .The basic process of binary array multiplication involves the AND operation of multiplicand and multiplier bits and subsequent addition. NOR gates are used instead of AND in accordance with the De Morgan's Law:

A.B = (A' + B')'

IV. Hardware Modification

To design 4 x 4 number we have a tendency to need sixteen AND gates, of that every AND gate consists of 6 semiconductor unit. a similar hardware will replaced by NOR gate that consists of solely four transistors .This reduction in hardware results into less power consumption.

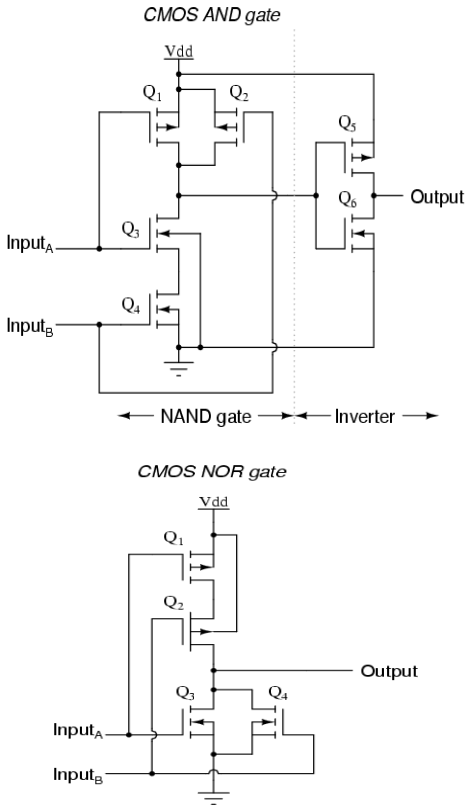


Figure 4: shows the circuit of CMOS AND gate and CMOS NOR gate.

Thus, for a m* n multiplier factor, the projected technique introduces m + n further inverters beside dynamic m*n AND gates to m*n NOR gates, effectively saving (m*n − (m + n)) inverters or 2*(m* n − (m+n)) transistors. Figure (3) shows projected multiplier factor style with the replacement of AND gate with a NOR gate in partial product of column bypassing multiplier, ensuing into demand of less no. of semiconductor than the traditional style. This reduction within the hardware results into less power consumption and ultimately help in a power improvement.

V. Result

1. The result of 32× 32 bit braun multiplier is evaluated. Its simulation result and Power analyzer summery is shown below the multiplication of 32× 32 bit numbers is done.

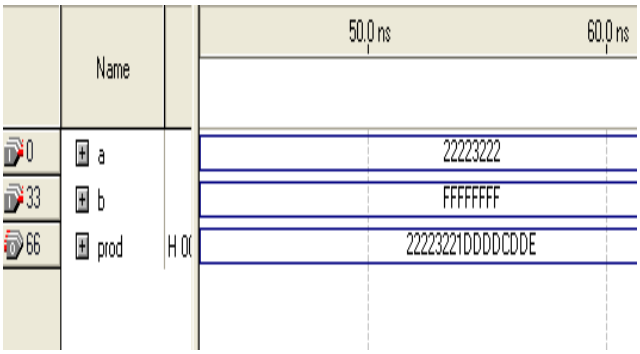


Figure 5: simulation result of 32× 32 bit braun multiplier

PowerPlay Power Analyzer Status	Successful - Mon May 12 20:56:18 2014
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	multiplier
Top-level Entity Name	multiplier
Family	Cyclone II
Device	EP2C5F256C6
Power Models	Final
Total Thermal Power Dissipation	124.65 mW
Core Dynamic Thermal Power Dissipation	10.88 mW
Core Static Thermal Power Dissipation	18.21 mW
I/O Thermal Power Dissipation	95.57 mW
Power Estimation Confidence	High: user provided sufficient toggle rate data

Figure 5: Power analysis of 32× 32 bit braun multiplier

2. The result of 32× 32 bit of column bypassing multiplier is evaluated. Its simulation result and Power analyzer summery is shown below the multiplication of 32× 32 bit numbers is done.

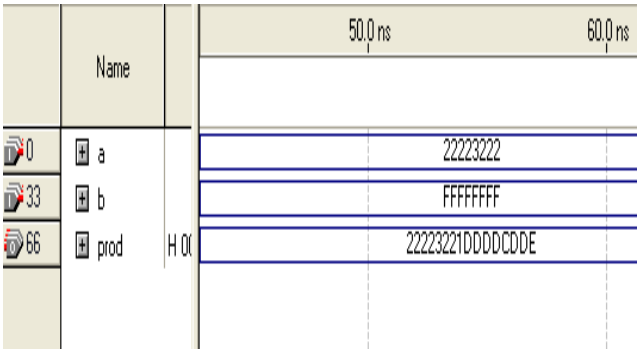


Figure 6: simulation result of 32× 32 bit column bypassing multiplier

PowerPlay Power Analyzer Status	Successful - Mon May 12 21:08:45 2014
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	multiplier
Top-level Entity Name	multiplier
Family	Cyclone II
Device	EP2C5F256C6
Power Models	Final
Total Thermal Power Dissipation	108.26 mW
Core Dynamic Thermal Power Dissipation	8.05 mW
Core Static Thermal Power Dissipation	18.17 mW
I/O Thermal Power Dissipation	82.03 mW
Power Estimation Confidence	High: user provided sufficient toggle rate data

Figure 6: Power analysis of 32× 32 bit column bypassing multiplier

VI. Conclusion

In this analysis work, a replacement approach for the look of parallel array multiplier factor has been steered. AND gates within the existing styles are replaced with NOR gates. By this modification in column bypassing multiplier factor, the ability consumption is reducing.

VII. Future Work

The changes in design of partial product of column bypassing multiplier will be implemented in modified column bypassing multiplier. This proposed work will be evaluated in future

VIII. References

[1] Jin-Tai Yan, Zhi-Wei Chen," Low-Cost Low-Power Bypassing-Based Multiplier Design", 978-1-4244-5309-2/10/$26.00 ©2010 IEEE

[2] J. T. Yan and Z. W. Chen, "Low-power multiplier design with row and column bypassing," IEEE International SOC Conference, pp.227-230, 2009.

[3] M. C. Wen, S. J. Wang and Y. M. Lin, "Low power parallel multiplier with column bypassing," IEEE International Symposium on Circuits and Systems, pp.1638-1641, 2005.

[4] J. Ohban, V. G. Moshnyaga, and K. Inoue, "Multiplier energy reduction through bypassing of partial products," IEEE Asia-Pacific Conference on Circuits and Systems, pp.13–17, 2002.

[5] J. Ohban, V. G. Moshnyaga, and K. Inoue, "Multiplier energy reduction through bypassing of partial products," IEEE Asia-Pacific Conference on Circuits and Systems, pp.13–17, 2002.

[6] J. Choi, J. Jeon and K. Choi, "Power minimization of functional units by partially guarded computation," International Symposium on Low-power Electronics and Design, pp.131-136, 2000

[7] T. Nishitani, "Micro-programmable DSP chip," 14th Workshop on Circuits and Systems, pp.279-280, 2001.

[8] T. Ahn and K. Choi, "dynamic operand interchange for low power," Electronics Letters, Vol. 33, no. 25, pp.2118-2120, 1997.

[9] A. Wu, "High performance adder cell for low power pipelined multiplier," IEEE International Symposium on Circuits and Systems, pp.57–60, 1996.